REMARKS

This Amendment responds to the Final Office Action mailed April 19, 2005 in the above-identified application. The foregoing Amendment involves only cancellation of non-elected claims. Accordingly, entry of the Amendment and allowance of the application are respectfully requested.

Claims 1-26 were previously pending in the application. Withdrawn claims 7-17 and 19-24 are canceled without prejudice or disclaimer. Accordingly, claims 1-6, 18, 25 and 26 are currently under consideration, with claims 1 and 18 being independent claims.

The Examiner has rejected claims 1 and 18 under 35 U.S.C. §103(a) as unpatentable over Amon et al. (U.S. 5,742,621) in view of Foland, Jr. (U.S. 5,412,669). Claims 2-6, 25 and 26 are rejected under 35 U.S.C. §103(a) as unpatentable over Amon et al. and Foland, Jr. in view of Benedetto et al. (article entitled "Soft-Output Decoding Algorithms in Iterative Decoding of Turbo Codes"). The rejections are respectfully traversed.

The Amon patent discloses a parallel data structure and a dedicated Viterbi shift-left instruction which minimize the number of clock cycles required for decoding a convolutionally encoded signal in a data processing system in software. The data structure and the Viterbi shift-left instruction reduce the number of clock cycles required for performing an add-compare-select butterfly operation (abstract). Fig. 4 of Amon illustrates assembly code for implementing the ACS butterfly in a digital signal processor in 14 clock cycles (col. 9, lines 24-36). Fig. 5 of Amon illustrates assembly code for implementing the ACS butterfly in a digital signal processor in 10 clock cycles (col. 9, lines 37-49). As shown in Figs. 4 and 5 of Amon, the ACS loop involves multiple instructions.

The Foland, Jr. patent describes an add-compare-select circuit in a sequence detector used with magnetic recording equipment (col. 17, lines 4-6). The abstract states that the entire add, compare and select process is accomplished in one cycle. However, a careful reading of Foland, Jr. indicates that a final result is not obtained in one cycle. "The result is not an accurate summation of the quantities but is an accurate depiction of which quantity is the least when compared to other quantities which are the result of a similar additive process" (col. 6, lines 39-42). Although "the X path is selected and the Y path is discarded, the actual value of the path metric at node Z has not

been calculated, since the carry bits from the current cycle... were not added in the calculation of the upper bit path metric. That step is performed on the next cycle..." (Figs. 12 and 13 and col. 16, lines 14-31) (see also col. 17, lines 40-46).

In contrast to Amon, claim 1 is directed to a method for processing signal values, wherein a single trellis instruction, including adding, subtracting, comparing and selecting operations, is executed by a digital signal processor in a single clock cycle of the digital signal processor. Amon contains no disclosure or suggestion of a trellis instruction that can be executed in a single clock cycle as claimed. The Amon operations require multiple clock cycles.

Foland, Jr. does not provide the teachings that are lacking in Amon. As described above, Foland, Jr. describes an add, compare and select circuit wherein a comparison result is obtained in one clock cycle and the sum of the quantities is determined on a subsequent clock cycle. The Foland, Jr. circuit would not be suitable for the present invention because the trellis state metrics are calculated on each clock cycle according to the present invention. The results of one calculation are used in the next calculation. The Foland, Jr. circuit does not provide summation results in one clock cycle and thus could not be utilized. Accordingly, the skilled person would not look to Foland, Jr. for an add, compare and select circuit. In summary, the add, compare and select circuit disclosed by Foland, Jr. does not perform a complete calculation in a single clock cycle as claimed. For these reasons, claim 1 is clearly and patentably distinguished over Amon in view of Foland, Jr.

Claims 2-6 depend from claim 1 and are patentable over Amon in view of Foland, Jr., taken individually or in combination with Benedetto, for at least the reasons discussed above in connection with claim 1. Benedetto does not provide the teachings that are lacking in Amon and Foland, Jr.

Claim 18 is similarly distinguished over Amon and Foland, Jr. In particular, neither Amon nor Foland, Jr. discloses or suggests a processor wherein the adders, the comparator and the data selector of an accelerator are configured to execute the adding, subtracting, comparing and selecting operations of a trellis instruction in a single clock cycle of the processor. For these reasons and for the reasons discussed above in connection with claim 1, claim 18 is clearly and patentably distinguished over Amon in view of Foland, Jr.

Claims 25 and 26 depend from claim 18 and are patentable over Amon and Foland, Jr., taken individually or in combination with Benedetto, for at least the reasons discussed above in connection with claims 1 and 18.

For the foregoing reasons, claims 1-6, 18, 25 and 26 are in condition for allowance, and withdrawal of the rejections is respectfully requested.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Dated: July 19, 2005

Respectfully submitted,

By William R. McClellan

William R. McClellan
Registration No.: 29,409
WOLF, GREENFIELD & SACKS, P.C.
Federal Reserve Plaza
600 Atlantic Avenue
Boston, Massachusetts 02210-2206
(617) 646-8000